Notice of Allowability	Application No. 09/819,198	Applicant(s) GAUTHIER ET AL.	
	Examiner Kandasamy Thangavelu	Art Unit 2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *April 14, 2005*.

2. ☒ The allowed claim(s) is/are *8-11 and 13*.

3. ☒ The drawings filed on *07 June 2001* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 28 March 2001
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☒ Other *PTO-1449 of 25 August 2003*.

DETAILED ACTION

Introduction

1. This communication is in response to the Applicants' communication dated April 14, 2005. Claims 1-4, 6, 8-11 and 13 were amended. Claims 5, 7 and 12 were canceled. Claims 14-17 were added. Claims 1-4, 6, 8-11 and 13-17 of the application are pending.

Drawings

2. The drawings submitted on June 7, 2001 are accepted.

Examiner's Amendment

3. Authorization for this examiner's amendment was given in two telephone conversations by Mr. Wasif Qureshi on June 7, 2005 and on June 21, 2005.

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to the applicants, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

4. In the Claims:

In amended Claims 1-4 and 6:

Delete claims 1-4 and 6.

In amended Claim 8, Lines 1-7, "A method for simulating an anti-resonance circuit of a section of a microprocessor, comprising:

simulating a load of the anti-resonance circuit;

simulating at least one high frequency capacitance of the anti-resonance circuit in parallel with the simulated load; and

simulating an intrinsic capacitance in parallel with the simulated load"

has been changed to

-- A computer implemented method for simulating an anti-resonance circuit of a section of a microprocessor, comprising:

simulating a load of the anti-resonance circuit;

simulating using a simulated transistor model, at least one high frequency capacitance of the anti-resonance circuit in parallel with the simulated load; and

simulating using a simulated capacitor model, an intrinsic capacitance of the section of the microprocessor in parallel with the simulated load--.

In Claims 14-17:

Delete claims 14-17.

A clean copy of the amended claims is attached.

Reasons for Allowance

5. Claims 8-11 and 13 of the application are allowed over prior art of record.

6. The following is an Examiner's statement of reasons for the indication of allowable subject matter:

The closest prior art of record shows:

(1) design of on-chip decoupling capacitance causes resonance oscillations in the power distribution network; modeling the resonance effects in the power supply network of CMOS ICs for predicting the resonance frequency and the damping factor of the CMOS ICs; increasing damping as a method to control resonance in the CMOS ICs (**Larsson,** "Resonance and damping in CMOS circuits with on-chip decoupling capacitance", IEEE 1998);

(2) an adaptive filter system for determining characteristics of an input signal and eliminating resonant and /or anti-resonant responses in an input; the system comprises a source of the input signal, at least two anti-resonance circuits coupled to the input source, means for determining the deviations of the anti-resonance frequencies of the anti-resonance circuits from the resonant frequencies of the input signal, means for cross correlating the output from at least one of the anti-resonance circuits with deviation and means for generating correction signals from the cross-correlation, the correction signals selectively varying the anti-resonant

frequencies of the anti-resonance circuits, so the anti-resonant frequencies correspond to the resonant frequencies of the input signal (**Jackson et al.,** U. S. Patent 3,808,370); and

(3) a chip antenna for use in mobile communication apparatus, the chip antenna having a plurality of resonance frequencies; the chip antenna comprises a base comprising at least one dielectric material and a magnetic material, at least one conductor provided with the base or on the surface of the base, and an anti-resonance circuit inserted in the immediate portion of the conductor and electrically connected in series; the anti-resonance circuit causes the conductor to resonate at the frequency corresponding to the length of the conductor; the anti-resonance circuit resonates at another frequency; the chip antenna can have resonance frequency corresponding to the length of the conductor and a frequency corresponding to the length from one end of the conductor to the position at which the anti-resonance circuit is connected (**Dakeya et al.,** U. S. Patent 6,075,491).

6.1 Applicants' first set of claims consists of Claims 8-11 and 13.

Independent Claim 8 is directed to a computer implemented method for simulating an anti-resonance circuit of a section of a microprocessor. The claim identifies the uniquely distinct features of:

"simulating a load of the anti-resonance circuit" and "simulating using a simulated transistor model, at least one high frequency capacitance of the anti-resonance circuit in parallel with the simulated load".

Because the closest prior art fails to teach or fairly suggest simulating a load of the anti-resonance circuit and simulating using a simulated transistor model, at least one high frequency capacitance of the anti-resonance circuit in parallel with the simulated load, as claimed by the Applicants, Claims 8-11 and 13 are deemed novel and allowable.

7. Any comments considered necessary by applicants must be submitted no later than the payment of the issue fee and, to avoid processing dela8ys, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 571-272-3717. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard, can be reached on 571-272-3749. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to TC 2100 Group receptionist: 571-272-2100.

K. Thangavelu
Art Unit 2123
June 21, 2005

LEO PICARD
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100